CONSTRUCTION ON

CEAS EPHAXIAL CROWNHMETHOD ON SISUESTRATIE

Patent Number:

JP1117017

Publication date:

1989-05-09

Inventor(s):

OGASAWARA KAZUTO

Applicant(s):

FUJITSU LTD

Requested Patent:

JP1117017

Application Number: JP19870274088 19871029

Priority Number(s):

IPC Classification: H01L21/203; H01L21/20

EC Classification:

EC Classification:

Equivalents:

Abstract

PURPOSE: To realize the epitaxial growth of a GaAs layer without generating defects, by interposing, on an Si substrate, a Ge/GaAs/Si distorted superlattice layer composed of twoatomic layers, and growing a GaAs thin layer at a low temperature.

CONSTITUTION:On an Si substrate 1, a superlattice layer is repeatedly subjected to epitaxial growth by a treating method capable of controlling the growth for every atomic layer. The superlattice layer is composed of a Si layer 4, a GaAs layer 3 on the layer 4, and a Ge layer 2 on the layer 3, each of which has even number of atomic layers. A Ge layer 5 whose number of atomic layer is larger than that of a Ge layer consituting the superlattice layer is subjected to epitaxial growth. A GaAs layer 6 with several tens of atomic layers is subjected to epitaxial growth at a first temperature. A GaAs layer 7 for element formation is subjected to epitaxial growth at a second temperature higher than the first temperature. Thereby enabling the epitaxial growth of a GaAs layer without generating defects.